ABSTRACT OF THE DISCLOSURE

A programmable logic controller with enhanced and extended the capabilities. A digital input filter implement filters with considerable less logic by simulating the action of a capacitor being driven by a constant current source whose output voltage is sensed by a comparator with a large amount of hysterisis. A pulse catch circuit captures the input pulse even though the update occurs between scan cycles. A pulse output controller includes a hardware pipeline mechanism to allow for smooth, hardware-controlled transitions from wave-form to wave-form. A free port link allows the user to control the port either manually or by operation of a user program. In order to provide higher performance for communication using PPI protocol, the PLC includes a built-in protocol. An n-bit modem protocol ensures data integrity without use of a parity type data integrity system. A hide instruction protects proprietary software by encrypting the sensitive code and decrypting the code during compilation and, thereafter, re-encrypting the code. A system function call allows the user to create and/or download new PLC functions and implement them as PLC operating system functions. An STL status function debugs programs during run-time and while the program is executing. A micro PLC arrangement provides compact size and efficiency.